Attorney Docket No. 15138US02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In the Application of:	)	
Pai	)	Electronically Filed
U.S. Serial No.: 10/736,125	)	December 13, 2010
Filed: 12/15/2003	)	
Examiner: Tseng	)	
Group Art Unit: 2184	)	
Confirmation No. 3609	)	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This is an appeal from the Office Action made Final mailed April 12, 2010 in which claims 18-30 were rejected. A Notice of Appeal was filed on August 12, 2010.

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I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine California 92618-3616, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-17 are cancelled without prejudice.

Claims 18-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee.

Claims 18-30 are appealed

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 18 is directed to a direct memory access controller, said direct memory access controller comprising (*Specification* at 12, Lines 18-19, Figure 4, DMA Engine 510):

a state logic machine for receiving a single command to provide a specified range of a plurality of

sequential data words, wherein the single command expressly states a starting address and an ending address of said specified range (*Specification* at 12, Lines 23-29, Figure 4, 605); and

a memory controller (*Specification* at 12, Line 19, Figure 4, 620) for fetching a first portion of the specified selectable range (*Specification* at 13, Lines 6-9) and a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion (*Specification* at 13, Lines 18-20), after the state logic receives the single command including the starting address and the ending address.

Claim 24 is directed to a method for fetching data words, said method comprising:

receiving a single command to provide a range of a plurality of sequential data words in a memory, wherein the command expressly states a starting at a beginning address and ending at an ending address of said range (*Specification* at 14, Lines 17-22);

fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of a predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer (*Specification* at 15, Lines 6-8);

storing the predetermined amount of data words that conclude with and precede the ending address in the local buffer (*Specification* at 15, Lines 9-10);

fetching, in the forward address order, at least one preceding portion of the range of sequential data

words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words (*Specification* 13, Lines 19-23); and

wherein a one of the preceding portions of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address (*Specification* at 14, Lines 28-32).

Claim 30 is directed to a system for decoding video data, said system comprising:

a memory for storing a packetized elementary stream, said packetized element stream comprising a plurality of packets (Figure 3, 505);

a start code table for storing starting addresses and ending addresses of said plurality of packets (Figure 3, 507);

a video decoder for decoding a particular one of the plurality of packets, wherein the video decoder looks up the starting addresses and the ending addresses of the particular one of the plurality of packets and issues a single command to fetch the packet, wherein the single command expressly includes a starting address and an ending address associated with the particular one of the plurality packets (Figure 2, 445); and

a direct memory access controller, said direct memory access controller comprising (*Specification* at 12, Lines 18-19, Figure 4, DMA Engine 510):

a state logic machine for receiving the single command (*Specification* at 12, Lines 23-29, Figure 4, 605); and

a memory controller (*Specification* at 12, Line 19, Figure 4, 620) for fetching a first portion of a range, said range comprising sequential data words from the

starting address to the ending address for the particular one of the plurality of packets (*Specification* at 13, Lines 6-9), and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion (*Specification* at 13, Lines 18-20), after the state logic receives the single command including the starting address and the ending address.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Rejection of claims 18-30 under 35 U.S.C. 102(e) as anticipated by Lee (U.S. Patent No. 6,842,219).

VII. ARGUMENT: CLAIM 18

Claim 18 was rejected under 35 U.S.C. 102(e) as being anticipated by Lee. Claim 18 is copied below:

> A direct memory access controller, said direct memory access controller comprising:
>
> a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words, wherein the single command expressly states a starting address and an ending address of said specified range; and
>
> a memory controller for fetching a first portion of the specified selectable range and a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command including the starting address and the ending address.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Assignee respectfully submits that the rejection to claim 18 is in error because each and every element as set forth in the claim are not found in Lee, either expressly or inherently.

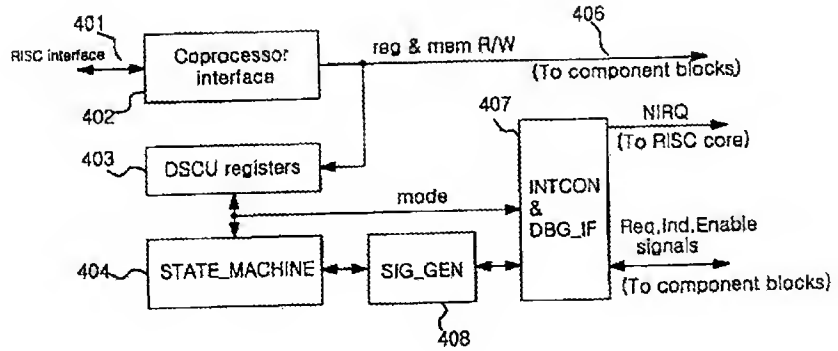
A. THE REJECTION TO CLAIM 18 SHOULD BE REVERSED BECAUSE LEE DOES NOT TEACH A "*STATE MACHINE FOR RECEIVING A COMMAND*"

Examiner has indicated that Lee teaches

> a state logic machine (fig. 4, decoding sequencing control unit DSCU 203a; fig. 2, DSCU 203a; fig. 9, state transition of DSCU 203a; note, each arc of the diagram represents a command for transition to another state) for receiving a single command (fig. 4, receiving commands from RISC interface 401; col. 10 line 33-36, data/address/control signals from RISC; fig. 6 coprocessor command for DSCU; col. 4, lines 27-29).

Final Office Action (FOA) at 3.

Appellant respectfully submits that the foregoing is in error. Lee, Figure 4, the DSCU 203a, is copied below:



Although the DSCU *includes* "state machine 404" and "co-processor interface 402" that interprets the coprocessor command data generated from RISC processor 207", the state machine 404 does not receive the commands.

It is first noted that even the DSCU 203a does not receive a command. The "co-processor interface 402" *interprets* the command *data* by using the data, address and control signals inputted/outputted through the RISC interface 401." None of data, addresses, and control signals, *per se*, are commands. For example, Lee does not teach that "co-processor interface 402" receives an op code.

Secondly, even if the "co-processor interface 402" is deemed to receive a command, the output of the co-processor interface 402 is not. Lee teaches that "[co-processor interface 402] decides whether the data is required for register read/write of a certain block or for DEC memory access [external to the DSCU], and thereafter generates appropriate *signals* to the blocks and distributes them." Lee, Col. 10, Lines 37-40. The hardwired signals that effectuate a read or write are not themselves considered commands. Therefore, even if the co-processor interface 402 is deemed to receive commands, no other unit in the DSCU 203a, including the state machine 404 receives them.

"Figure 9 is a view illustrating the state transition used for DSCU". Lee, Col. 4, Lines 35-38. Examniner has indicated that "each arc of the diagram represents a command for transition to another state". Appellant submits that the foregoing is also in error.

Figure 9 shows a set of states, wherein the arcs represents changes in states. The annotations on the arcs are not commands, but rather conditions. At a particular

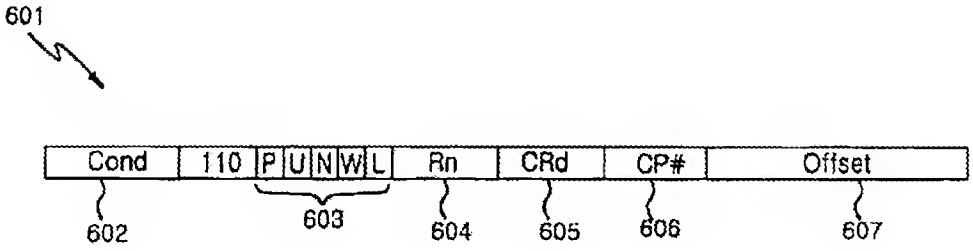
state, when a condition occurs, the respective arc path is followed to the next state. Those of ordinary skill in the art will recognize that changes from one state to another state do not require commands. For example, the behavior of logic elements such as flip-flops are often described using state diagrams. However, no commands are needed to change states.

Therefore, Lee does not teach a "state machine for receiving a command". Accordingly, for at least the foregoing reason, the rejection to claim 1 should be REVERSED.

B. THE REJECTION TO CLAIM 18 SHOULD BE REVERSED BECAUSE LEE DOES NOT TEACH A "SINGLE COMMAND TO *PROVIDE A SPECIFIED RANGE OF A PLURALITY OF SEQUENTIAL DATA WORDS*"

Examiner has indicated that the foregoing is taught at Lee, col. 4, lines 27-29, col. 11, lines 15-19, the "address range of external memory to be accessed", and lines 62-65, noting that "DSCU carries sequential sequence control of MPEG stream, and col. 12, lines 38-41, noting "macroblocks as data words". FOA at 3.

Col. 4, lines 27-29 states that "Fig. 6 is a view illustrating the structure of a coprocessor command used for external memory access of CODEC blocks in DSCU". Lee, Figure 6 is copied below:



It is first noted that the foregoing is a *co-processor* command, but not a *co-processor interface* command. The co-processor and co-processor interface (in the DSCU) are different units. Examiner does not allege that the co-processor is the claimed "state machine". The VDEC 203 that contains the DSCU 203a that Examiner reads the limitation on, does not even receive this command.

Lee teaches that VDEC 203 "should inform to RISC processor 207 by using a command 601, and then RISC processor 207 can access data through main bus 211." Col. 11, Lines 15-19. Thus, instead of VDEC 203 "receiving" the command 601, VDEC actually issues command 601 for the RISC processor 207.

Furthermore, command 601 does not include the capability to specify a range of data words. Field "CRd" is a four bit values that merely identifies *which* memory is used. Col. 11, lines 23-24. Mere identification of a memory is not specification of a range of data words.

However, even if, arguendo, identification of a memory is held to be specification of a range being the first data word to the last data word of the identified memory, Assignee respectfully submits that Lee's identification of a memory, CRd is not "a single command to provide" all of the words from the first data word of the identified memory to the last word of the identified memory.

Turning now to col. 11, lines 62-65, the foregoing merely states that "DSCU 203a basically carries out a sequential sequence control…". However, Lee does not indicate that the foregoing is caused by a single instructions, and does not indicate that the foregoing "sequence control" is "providing a specified range of a plurality of sequential data words".

Finally, the Office Action of 9/11/09 at 12 stated that "as MPEG stream decoding control, the DSCU receives a command to fetch MPEG stream as sequential data words for decoding. The specified selectable range is the fetch size of each MPEG stream fetch from external memory. The MPEG stream is the sequential data words."

Appellant maintains that the foregoing is in error. Nothing in Lee indicates that the foregoing is occurs by a single command. Moreover, the foregoing assumes that the MPEG stream is static in memory. Lee does not indicate that this is the case. Moreover, it is often not the case. For example, the MPEG stream is often received from the internet or other communication network. Lee even acknowledges this. See Col. 1. When the video is played in real time, for example, streaming video, the fetch size and ending address of the MPEG stream would be indeterminate.

Accordingly, for at least the foregoing reason, Lee does not teach the claimed "single command to provide a specified range of a plurality of sequential data words."

C. LEE DOES NOT TEACH "WHEREIN THE SINGLE COMMAND EXPRESSLY STATES A *STARTING ADDRESS* AND AN *ENDING ADDRESS*"

Even if Lee is deemed to teach single command to provide a specified range of a plurality of sequential data words, Lee does not teach "wherein the single command expressly states a starting address and an ending address". For example, clearly command 601 does not include the capability to expressly state a starting address and an ending address.

Examiner has indicated that the foregoing is taught at col. 10, lines 41-46 and col. 13, lines 45-52. Col. 10,

lines 41-46, states that "DSCU register 403 is for storing the data related to various contol signals generated in case of register and memory read/write 406. And at the time of read/write of the DEC memory 203f, which is a local memory, it stores the control data for assigning the start address and the the end address of the memory to be used."

The foregoing actually demonstrates that it is not "a single command" that "expressly states a starting address and an ending address". First, values in DSCU register 406 are not part of a command, itself. Secondly, DSCU register does not *expressly* state a starting address and an ending address, but merely "stores the *control data for assigning* the start address and the the end address".

Examiner has indicated that a "given range must have associated starting and ending addresses". However, even if this is the case, the starting and ending addresses do not have to be known, can be implied, or abstracted. Also, even a range has an express starting and ending address, the foregoing do not have to be in the command.

Accordingly, Appellant respectfully submits that Lee does not teach "wherein the single command expressly states a starting address and an ending address". Accordingly, for at least the foregoing reason, Appellant respectfully requests that the rejection to claim 18 be REVERSED.

D. LEE DOES NOT TEACH "FETCHING A FIRST PORTION OF THE SPECIFIED SELECTABLE RANGE AND A SECOND PORTION OF THE SPECIFIED SELECTABLE RANGE"

Examiner has also indicated that Lee teaches "a memory controller (fig. 11, buffer controller 1113 of variable length decoder VLD 203ba; fig. 2, VLD 203ba; fig. 12 reversal logic) for fetching a first portion (fig. 11, a

portion of VLD input buffer 1112; col. 13 lines 27-35, fetch into barrel shift 1104 to lower 32 bit) of the specified selectable range and a second portion (fig. 11, a next portion of VLD input buffer 1112; col. 13, lines 27-35, move lower 32 bit to higher 32 and fetch new lower 32 bit) of the range after fetching the first portion". Office Action at 8.

Appellant notes that "the range" takes antecedent basis from "a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words". The Final Office Action reads the "state logic machine" onto DSCU, and the command onto 601. Lee does not teach buffer controller 1113 fetches any range specified in command 601 that is ever received by state machine 404, even if command 601 is deemed to teach a specified range, and state machine 404 is deemed to receive command 601.

Accordingly, Appellant respectfully requests that the rejection to claim 18 be REVERSED.

E. LEE DOES NOT TEACH "A SECOND PORTION OF THE SPECIFIED SELECTABLE RANGE AFTER FETCHING THE FIRST PORTION, WHEREIN THE SECOND PORTION OF THE RANGE HAS A LOWER ADDRESS THAN THE FIRST PORTION"

The Final Office Action indicates that the foregoing is taught at "col. 13, lines 27-35, barrel shifter 1104, the new fetch is always shift into lower 32 bit address".

Appellant respectfully submits that the foregoing is in error. Those of ordinary skill in the art would deem a "lower address" to be the address that the second portion is fetched *from*.

Accordingly, Appellant respectfully requests that the rejection to claim 18 be REVERSED.

F. DEPENDENT CLAIMS 19-23 AND 29

Additionally, claims 19-23, 29, and 30 depend on claim 18. Accordingly, Appellant respectfully requests reversal of these rejections, as well.

VIII. ARGUMENT: CLAIM 20

Claim 20 was rejected as anticipated by Lee. Claim 20 is dependent on claim 18. The limitations of claims 20 are copied below:

> 20. (Previously Presented) The direct memory access controller of claim 18, further comprising:
>
> a local buffer for storing the first and second portions in a forward address order, said local buffer comprising a plurality of data words.

The Final Office Action at 9 indicates that "a local buffer" is taught at col. 6, line 58-60, "cache memory" and Fig. 16, DBC 203f. The foregoing is in error.

However, Lee does not teach that either element store "the first and second portions".

Even if, *arguendo*:

Lee teaches "a first portion (fig. 11, a portion of **VLD input buffer** 1112; col. 13 lines 27-35, fetch into barrel shift 1104 to lower 32 bit) of the specified selectable

range and a second portion (fig. 11, a next portion of **VLD input buffer** 1112; col. 13, lines 27-35, move lower 32 bit to higher 32 and fetch new lower 32 bit)"

Lee does not teach the foregoing "first portion" and "second portion" would not be stored in either the DBC_MEM 203f or the RISC cache.

Accordingly, Appellant respectfully requests that the rejection to claim 20 be REVERSED.

IX. ARGUMENT: CLAIM 24

Claim 24 was rejected under 35 U.S.C. 102 as anticipated by Lee. Claim 24 is copied below:

> A method for fetching data words, said method comprising:
>
> receiving a single command to provide a range of a plurality of sequential data words in a memory, wherein the command expressly states a starting at a beginning address and ending at an ending address of said range;
>
> fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of a predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer;
>
> storing the predetermined amount of data words that conclude with and precede the ending address in the local buffer;
>
> fetching, in the forward address order, at least one preceding portion of the range of sequential data words, wherein each of the

preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein a one of the preceding portions of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address.

Appellant respectfully incorporates the arguments in Section VII and requests that the rejection to claim 24 and dependent claims 25-28 be REVERSED.

Additionally, claim 24 recites, among other limitations, "wherein a one of the preceding portions of the range of sequential data words comprises the starting address, *truncating those data words that precede the beginning address*."

The Final Office Action indicates that the foregoing is taught at col. 10, lines 49-55, backward decoding; col. 15, lines 49-52, MPEG-4 rewinding and error resilience, the point of error has beginning address.

Appellant respectfully submits that the foregoing is in error. It is noted that "the starting address" takes antecedent basis to "wherein the command expressly states a starting at a beginning address and ending at an ending address of said range".

Lee does not teach that that the "wherein the command expressly states a starting at a beginning address" wherein "point of error" is the beginning address. Moreover, if the point of error is the beginning address, Lee does not teach truncating *prior* to the "point of error".

Accordingly, Lee does not teach "wherein a one of the preceding portions of the range of sequential data words

comprises the starting address, *truncating those data words that precede the beginning address.*"

Accordingly, Appellant requests that the rejection to claim 24 and dependent claims 25-27 be REVERSED.

X. ARGUMENT: CLAIM 30

Claim 30 was rejected under 35 U.S.C. 102 as anticipated by Lee. Appellant respectfully incorporates the arguments in Section VII and requests that the rejection to claim 30 be REVERSED.

XI. CONCLUSION

For at least the foregoing reasons, the Board of Patent Appeals and Interferences is respectfully requested to REVERSE the rejections to claims 18-30. The Commissioner is hereby authorized to charge any fees for any action requested herein to deposit account 13-0017.

Dated: December 13, 2010

Respectfully submitted,

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CLAIMS APPENDIX

18. (Previously Presented) A direct memory access controller, said direct memory access controller comprising:

a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words, wherein the single command expressly states a starting address and an ending address of said specified range; and

a memory controller for fetching a first portion of the specified selectable range and a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command including the starting address and the ending address.

19. (Previously Presented) The direct memory access controller of claim 18, wherein the memory controller fetches the first portion of the range and the second portion of the range in a forward address order.

20. (Previously Presented) The direct memory access controller of claim 18, further comprising:

a local buffer for storing the first and second portions in a forward address order, said local buffer comprising a plurality of data words.

21. (Previously Presented) The direct memory access controller of claim 20, wherein the plurality of data words

of the local buffer are narrower in width than the sequential data words.

22. (Previously Presented) The direct memory access controller of claim 20, further comprising:

a port for transmitting the contents of the plurality of data words of the local buffer in a reverse address order.

23. (Previously Presented) The direct memory access controller of claim 22, further comprising:

at least one multiplexer for reversing the bit positions of contents of at least one of the data words of the local buffer.

24. (Previously Presented) A method for fetching data words, said method comprising:

receiving a single command to provide a range of a plurality of sequential data words in a memory, wherein the command expressly states a starting at a beginning address and ending at an ending address of said range;

fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of a predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer;

storing the predetermined amount of data words that conclude with and precede the ending address in the local buffer;

fetching, in the forward address order, at least one preceding portion of the range of sequential data words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein a one of the preceding portions of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address.

25. (Previously Presented) The method of claim 24, further comprising:

loading the portion and the at least one preceding portions of the sequential data words into the local buffer.

26. (Previously Presented) The method of claim 25, further comprising:

reversing the portion and the at least one preceding portions of the range of sequential data words.

27. (Previously Presented) The method of claim 26. further comprising:

reversing the truncated one of the preceding portions of the range of sequential data words that comprises the beginning address.

28. (Previously Presented) The direct memory access controller of claim 18, wherein the first portion and the second portion are adjacent to each other.

29. (Previously Presented) The direct memory access controller of claim 18, wherein the specified selectable range of the plurality of sequential data words is less than a memory storing the plurality of sequential data words.

30. (Previously Presented) A system for decoding video data, said system comprising:

a memory for storing a packetized elementary stream, said packetized element stream comprising a plurality of packets;

a start code table for storing starting addresses and ending addresses of said plurality of packets;

a video decoder for decoding a particular one of the plurality of packets, wherein the video decoder looks up the starting addresses and the ending addresses of the particular one of the plurality of packets and issues a single command to fetch the packet, wherein the single command expressly includes a starting address and an ending address associated with the particular one of the plurality packets; and

a direct memory access controller, said direct memory access controller comprising:

a state logic machine for receiving the single command; and

a memory controller for fetching a first portion of a range, said range comprising sequential data words from the starting address to the ending address for the particular one of the plurality of packets, and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the

single command including the starting address and the ending address.

EVIDENCE APPENDIX

There are no pages in this Appendix.

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.